SPECIFICATION AMENDMENTS

Please replace the paragraph beginning on page 4, line 23 with the following replacement paragraph:

Figure 1 is a block diagram of both a conventional differential PLL and a differential PLL including a charge pump in accordance with an embodiment of the invention.

Please replace the paragraph beginning on page 5, line 16 with the following replacement paragraph:

The current sources formed from transistor pairs N3/N4 and N7/N8 bias differential NMOS transistor pairs N1/N2 and N5/N6 ~~N5/N7~~, respectively. Thus, each differential pair will conduct a current Icp. This current will be conducted virtually entirely by one transistor or another within each differential pair depending upon the relative values of the differential voltages biasing the transistor gates. For example, the differential up voltage comprised of an up positive component and an up negative (UPN) component biases the gates of transistors N1 and N2, respectively. Similarly, a differential down voltage comprised of a differential down positive (DNP) component and a differential down negative (DNN) component biases the gates of transistors N6 and N5, respectively. The current switching performed by each differential pair may be further explained with respect to Figure 3, which illustrates the up and down differential voltage waveforms.